CLAIM AMENDMENTS

1. (Currently Amended) A method comprising:

detecting that a processor's frequency has changed in response to processor cooling;

generating an interrupt in response to the detection of the frequency change; [[and]]

determining whether the performance state of the processor is going to be a lower performance state [[or a higher performance state]]; and

changing the processor's frequency and then the processor's voltage if the performance state of the processor is going to be the lower performance state.

2. (Original) The method of claim 1 including providing an interrupt to an operating system.

3. (Original) The method of claim 1 including reading the performance state of the processor in response to the interrupt.

4. (Original) The method of claim 3 including determining a new performance state.

5. (Original) The method of claim 4 including scheduling a bandwidth allocation.

6. (Original) The method of claim 2 including setting up a periodic timer.

7. (Original) The method of claim 6 including monitoring the processor temperature at periodic intervals.

8. (Original) The method of claim 1 including detecting a high temperature or a low temperature interrupt and reading the processor performance state in response to the detection of a high temperature or a low temperature interrupt.

9. (Original) The method of claim 1 wherein detecting a frequency change includes detecting a processor phase locked loop event.

10.   (Original) The method of claim 1 including using hardware controlled throttling.

11.   (Currently Amended) An article comprising a medium storing instructions [[to]] that, if executed, enable a processor-based system to:

> detect that a processor's frequency has changed in response to processor cooling;
>
> generate an interrupt in response to the detection of the frequency change; [[and]]
>
> determine whether the performance state of the processor is going to be a lower

performance state [[or a higher performance state]]; and

> change the processor's frequency and then the processor's voltage if the

performance state of the processor is going to be the lower performance state.

12.   (Currently Amended) The article of claim 11 further storing instructions [[to]] that, if executed, enable a processor-based system to provide an interrupt to an operating system.

13.   (Currently Amended) The article of claim 11 further storing instructions [[to]] that, if executed, enable a processor-based system to read the performance state of the processor in response to the interrupt.

14.   (Currently Amended) The article of claim 13 further storing instructions [[to]] that, if executed, enable a processor-based system to determine a new performance state.

15.   (Currently Amended) The article of claim 14 further storing instructions [[to]] that, if executed, enable a processor-based system to schedule a bandwidth allocation.

16.   (Currently Amended) The article of claim 12 further storing instructions [[to]] that, if executed, enable a processor-based system to set up a periodic timer.

17.   (Currently Amended) The article of claim 16 further storing instructions [[to]] that, if executed, enable a processor-based system to monitor the processor temperature at periodic intervals.

18.   (Currently Amended) The article of claim 11 further storing instructions [[to]] that, if executed, enable a processor-based system to detect a high temperature or a low

temperature interrupt and read the processor performance state in response to the detection of a high temperature or a low temperature interrupt.

19.   (Currently Amended) The article of claim 11 further storing instructions [[to]] that, if executed, enable a processor-based system to detect a processor phase locked loop event.

20.   (Currently Amended) The article of claim 11 further storing instructions [[to]] that, if executed, enable a processor-based system to use hardware controlled throttling.

21.   (Currently Amended) A system comprising:
           a processor;
           a temperature sensor coupled to said processor; and
           a storage storing instructions that enable the processor to detect that the
processor's frequency has changed in response to processor cooling, generate an interrupt in response to detection of the frequency change, [[and]] determine whether the performance state of the processor is going to be a lower performance state [[or a higher performance state]], and change the processor's frequency and then the processor's voltage if the performance state of the processor is going to be the lower performance state.

22.   (Original) The system of claim 21 including a storage storing an operating system, said interrupt being provided to the operating system.

23.   (Original) The system of claim 21 wherein said storage stores instructions that enable the processor to read the performance state of the processor in response to an interrupt.

24.   (Original) The system of claim 21 wherein said processor determines a new performance state.

25.   (Original) The system of claim 24 wherein said storage stores instructions that enable the processor to schedule a bandwidth allocation.

26.   (Original) The system of claim 22 wherein said storage stores instructions that enable the processor to set up a periodic timer.

27. (Original) The system of claim 26 wherein said storage stores instructions that enable the processor to monitor the processor temperature at periodic intervals.

28. (Original) The system of claim 21 wherein said storage stores instructions that enable the processor to detect a high temperature or a low temperature interrupt and read the processor performance state in response to the detection of a high temperature or a low temperature interrupt.

29. (Original) The system of claim 21 wherein said storage stores instructions that enable the processor to detect a processor phase locked loop event.

30. (Original) The system of claim 21 including hardware controlled throttling.

31. (Currently Amended) The method of claim 1 including [[selectively changing the processor's frequency and then the processor's voltage when the performance state of the processor is going to be the lower performance state and]]

determining whether the performance state of the processor is going to be a higher performance state; and

changing the processor's voltage and then the processor's frequency [[when]] if the performance state of the processor is going to be the higher performance state.

32. (Currently Amended) The article of claim 11 further storing instructions [[to]] that, if executed, enable a processor-based system to [[selectively change the processor's frequency and then the processor's voltage when the performance state of the processor is going to be the lower performance state and]]

determine whether the performance state of the processor is going to be a higher performance state; and

change the processor's voltage and then the processor's frequency [[when]] if the performance state of the processor is going to be the higher performance state.

33. (New) A method comprising:

detecting that a processor's frequency has changed in response to processor cooling;

generating an interrupt in response to the detection of the frequency change;

determining whether the performance state of the processor is going to be a higher performance state; and

changing the processor's voltage and then the processor's frequency if the performance state of the processor is going to be the higher performance state.

34. (New) The method of claim 33 including providing an interrupt to an operating system.

35. (New) The method of claim 33 including reading the performance state of the processor in response to the interrupt.

36. (New) The method of claim 35 including determining a new performance state.

37. (New) The method of claim 36 including scheduling a bandwidth allocation.

38. (New) The method of claim 34 including setting up a periodic timer.

39. (New) The method of claim 34 including monitoring the processor temperature at periodic intervals.

40. (New) The method of claim 33 including detecting a high temperature or a low temperature interrupt and reading the processor performance state in response to the detection of a high temperature or a low temperature interrupt.

41. (New) The method of claim 33 wherein detecting a frequency change includes detecting a processor phase locked loop event.

42. (New) The method of claim 33 including using hardware controlled throttling.

43. (New) An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

detect that a processor's frequency has changed in response to processor cooling;

generate an interrupt in response to the detection of the frequency change;

determine whether the performance state of the processor is going to be a higher performance state; and

change the processor's voltage and then the processor's frequency if the performance state of the processor is going to be the higher performance state.

44. (New) The article of claim 43 further storing instructions that, if executed, enable a processor-based system to provide an interrupt to an operating system.

45. (New) The article of claim 43 further storing instructions that, if executed, enable a processor-based system to read the performance state of the processor in response to the interrupt.

46. (New) The article of claim 45 further storing instructions that, if executed, enable a processor-based system to determine a new performance state.

47. (New) The article of claim 46 further storing instructions that, if executed, enable a processor-based system to schedule a bandwidth allocation.

48. (New) The article of claim 44 further storing instructions that, if executed, enable a processor-based system to set up a periodic timer.

49. (New) The article of claim 48 further storing instructions that, if executed, enable a processor-based system to monitor the processor temperature at periodic intervals.

50. (New) The article of claim 43 further storing instructions that, if executed, enable a processor-based system to detect a high temperature or a low temperature interrupt and read the processor performance state in response to the detection of a high temperature or a low temperature interrupt.

51. (New) The article of claim 43 further storing instructions that, if executed, enable a processor-based system to detect a processor phase locked loop event.

52. (New) The article of claim 43 further storing instructions that, if executed, enable a processor-based system to use hardware controlled throttling.

53.   (New) A system comprising:

a processor;

a temperature sensor coupled to said processor; and

a storage storing instructions that enable the processor to detect that the processor's frequency has changed in response to processor cooling, generate an interrupt in response to detection of the frequency change, determine whether the performance state of the processor is going to be a higher performance state, and change the processor's voltage and then the processor's frequency if the performance state of the processor is going to be the higher performance state.

54.   (New) The system of claim 53 including a storage storing an operating system, said interrupt being provided to the operating system.

55.   (New) The system of claim 53 wherein said storage stores instructions that enable the processor to read the performance state of the processor in response to an interrupt.

56.   (New) The system of claim 53 wherein said processor determines a new performance state.

57.   (New) The system of claim 56 wherein said storage stores instructions that enable the processor to schedule a bandwidth allocation.

58.   (New) The system of claim 54 wherein said storage stores instructions that enable the processor to set up a periodic timer.

59.   (New) The system of claim 58 wherein said storage stores instructions that enable the processor to monitor the processor temperature at periodic intervals.

60.   (New) The system of claim 53 wherein said storage stores instructions that enable the processor to detect a high temperature or a low temperature interrupt and read the processor performance state in response to the detection of a high temperature or a low temperature interrupt.

61.   (New) The system of claim 53 wherein said storage stores instructions that enable the processor to detect a processor phase locked loop event.

62.   (New) The system of claim 53 including hardware controlled throttling.